VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

[0025] FIGS. 15-17 are cross-sectional views of [a prior art wirebonded] an adhesive coated lead finger of a LOC semiconductor assembly formed by the inversion method of the present invention;

IN THE CLAIMS:

26. (Amended) The semiconductor substrate of claim 7, wherein said at least one adhesive patch comprises at least one lateral edge exhibiting an angle of repose of [at least] approximately 20 degrees.

27. (Amended) The semiconductor substrate of claim 7, wherein said at least one adhesive patch comprises at least one trailing edge exhibiting an angle of repose of [at least] approximately 13 degrees.

28. (Amended) The semiconductor substrate of claim 7, wherein said at least one adhesive patch comprises at least one leading edge exhibiting an angle of repose of [at least] approximately 20 degrees.

29 (Cancelled) The semiconductor substrate of claim 7, wherein said at least one adhesive patch comprises a height-to-width ratio of at least approximately 3 to 1.

38. (Amended) The flip-chip of claim 15, wherein said at least one conductive bump comprises at least one lateral edge exhibiting an angle of repose of [at least] approximately 20 degrees.

39. (Amended) The flip-chip of claim 15, wherein said at least one conductive bump comprises at least one trailing edge exhibiting an angle of repose of [at least] approximately 12 degrees.

40. (Amended) The flip-chip of claim 15, wherein said at least one conductive bump comprises at least one leading edge exhibiting an angle of repose of [at least] approximately 20 degrees.

46. (Twice amended) A semiconductor substrate including at least one laterally unconstrained adhesive patch comprised of a viscous adhesive material exhibiting a stable, self-supporting shape, the at least one adhesive patch including a first surface adjacent and supported from beneath by said semiconductor substrate and a second smaller, exposed surface opposite said first surface, said second smaller, exposed surface exhibiting a generally planar portion over a substantial portion thereof.

48. (Twice amended) The semiconductor substrate of claim 46, wherein said at least one adhesive patch comprises at least one lateral edge exhibiting an angle of repose of [at least] approximately 20 degrees.

49. (Twice amended) The semiconductor substrate of claim 46, wherein said at least one adhesive patch comprises at least one trailing edge exhibiting an angle of repose of [at least] approximately 13 degrees.

50. (Twice amended) The semiconductor substrate of claim 46, wherein said at least one adhesive patch comprises at least one leading edge exhibiting an angle of repose of [at least] approximately 20 degrees.

51. (Cancelled) The semiconductor substrate of claim 46, wherein said at least one adhesive patch exhibits a height-to-width ratio of at least approximately 3 to 1.

59. (Twice amended) The flip-chip of claim 57, wherein said at least one conductive bump comprises at least one lateral edge exhibiting an angle of repose of [at least] approximately 20 degrees.

60. (Twice amended) The flip-chip of claim 57, wherein said at least one conductive bump comprises at least one trailing edge exhibiting an angle of repose of [at least] approximately 13 degrees.

61. (Twice amended) The flip-chip of claim 57, wherein said at least one conductive bump comprises at least one leading edge exhibiting an angle of repose of [at least] approximately 20 degrees.